

What is claimed is:

1. A power-up circuit for use in a semiconductor memory device, comprising:

5 a power supply voltage level follower unit for outputting a first bias voltage and a second bias voltage which increase or decrease in proportion to a power supply voltage;

 a first power supply voltage detecting unit for
10 detecting that the power supply voltage becomes a first critical voltage level of the power supply voltage corresponding to a threshold voltage of an NMOS transistor in response to the first bias voltage;

 a second power supply voltage detecting unit for
15 detecting that the power supply voltage becomes a second critical voltage level of the power supply voltage corresponding to a threshold voltage of a PMOS transistor in response to the second bias voltage; and

 a summation unit for performing a logic operation to a
20 first detect signal outputted from the first power supply voltage detecting unit and a second detect signal outputted from the second power supply voltage detecting unit to thereby output a confirmation signal, wherein the confirmation signal is activated when the power supply voltage satisfies both of
25 the first and second critical voltage levels.

2. The power-up circuit as recited in claim 1, further

includes a buffering unit for buffering the confirmation signal outputted from the summation unit to thereby output a power-up signal.

5 3. The power-up circuit as recited in claim 1, wherein the power supply voltage level follower unit includes a first load element, a second load element and a third load element, all connected between the power supply voltage and a ground voltage in series, for outputting the first bias voltage to a
10 first common node between the first load element and the second load element and outputting the second bias voltage to a second common node between the second load element and the third load element.

15 4. The power-up circuit as recited in claim 1, wherein the power supply voltage level follower unit includes:

 a first power supply voltage level follower unit having a first load element and a second load element connected in series between the power supply voltage and a ground voltage;

20 and

 a second power supply voltage level follower unit having a third load element and a fourth load element connected in series between the power supply voltage and the ground voltage.

25 5. The power-up circuit as recited in claim 1, wherein the first power supply voltage detecting unit includes:

 a first load element connected between the power supply

voltage and a first node;

an NMOS transistor connected between the first node and a ground voltage for receiving the first bias voltage through a gate of the NMOS transistor; and

5 a first inverter connected to the first node.

6. The power-up circuit as recited in claim 5, wherein the first load element is embodied as a P-channel metal oxide semiconductor (PMOS) transistor connected between the power supply voltage and the first node and receives the ground voltage through a gate of the PMOS transistor.

7. The power-up circuit as recited in claim 5, wherein the second power supply voltage detecting unit includes:

15 a second load element connected between the ground voltage and a second node;

a PMOS transistor connected between the second node and the power supply voltage for receiving the second bias voltage through a gate of the PMOS transistor;

20 a second inverter connected to the second node; and

a third inverter for receiving an outputted signal from the second inverter.

8. The power-up circuit as recited in claim 7, wherein the second load element is embodied as an NMOS transistor connected between the ground voltage and the second node and receives the power supply voltage through a gate of the NMOS

transistor.

9. The power-up circuit as recited in claim 7, wherein the summation unit includes:

5 a NAND gate for receiving the first detect signal and the second detect signal; and

 a fourth inverter for receiving an outputted signal from the NAND gate.

10 10. The power-up circuit as recited in claim 1, wherein the summation unit includes a NOR gate for receiving the first detect signal and the second detect signal.

15 11. The power-up circuit as recited in claim 2, wherein the buffering unit includes buffers connected in serial for receiving the confirmation signal.